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**UNITED STATES PATENT APPLICATION**

*of*

**Pravas Pradhan**

*and*

**Jianhong Ju**

*for a*

**CURRENT TRANSFER LOGIC**

## CURRENT TRANSFER LOGIC

### BACKGROUND OF THE INVENTION

#### *Field of the Invention*

5 The present invention relates to sending logic signals over terminated transmission lines, and more particularly to sending differential signals over transmission lines.

#### *Background Information*

10 Sending logic (and analog) signals over transmission lines while maintaining the fidelity by impedance matching of such signals has been of interest in many technical fields, especially in communications and computer systems, for many years. This area has become increasingly important as system speeds increase and power dissipation requirements decrease.

15 In logic and computer systems transmission line drivers typically began by transmitting unipolar logic (voltage) signals over matched transmission lines. Types of transmission lines used in such systems include, but not limited to, single and paired wires, twisted pairs, shielded twisted pairs, flat cables, flat cables with a ground shield, and coaxial. The terminating resistor, equal to the line's characteristic impedance, is connected across the distant end of the transmission line between the signal and the return lines. The 20 matching substantially eliminates reflections or ringing when the loading of the receiving circuitry impedance is one or more orders of magnitude higher than the characteristic impedance at the signal frequencies.

FIG. 1 shows a prior art logic voltage signal 10 driving a transmission line 12. When terminated with the lines characteristic impedance  $R_t$ , substantially the voltages

signal 10 is reproduced 12 across  $R_t$ . The return current will contribute to a noise signal  $V_n$  as will electrostatically and electromagnetically coupled signals from fast changing voltage and current signals in nearby circuits. Power dissipation, for example +3.3 V across a 50 ohm termination, speeds and noise  $V_n$  continue to limit the uses of driving 5 voltage signals.

Older, slower systems built around three and five volt logic operated well sending and receiving three and five volt signals over matched transmission lines. But as speeds increased and more circuitry is placed on chips, difficulties in driving capacitance, noise, jitter and power levels become issues that have spawned other techniques.

10 One improvement was to reduce the voltage signal levels, and to use differential voltage drivers and receivers. But, the same issues remain albeit at a lower level.

It has been recognized that current driving techniques may have a number of advantages with respect to speed, power dissipation, noise, and jitter. FIG. 2 illustrates one 15 advantage comparing a low voltage differential signal (LVDS)  $V_s$  driver and a current transfer logic (CTL)  $I_s$  driver. The analysis assumes that the receiving end of the transmission line senses voltage for the LVDS and current for the CTL circuit. In one case, an LVDS driver results in 3.5 mA of current into the line, or a voltage at the driver of 350mV. These levels are needed because there will be voltage loss along the line and the 20 receiver may receive only 100mV. The lost 250 mV represents a noise margin at the driver and attenuation due to the transmission line. Any other any noise contributions will further reduce that margin. For the CTL, a current,  $I_s$ , is sent, and, assuming good 25 quality transmission lines, and using Kirchoff's current (or charge) law, that DC current will be received at the receiver. So, a reduced current can be used with CTL resulting in substantially lower noise and power dissipation. Further, an effect of the reduced current, from FIG. 2, is that the  $dv/dt$  for the CTL is shorter than the  $dv/dt$  edge for  $V_s$  (with the same slopes) resulting in higher speed for the CTL circuit, since the signals reach their half way point faster. Moreover, for the same speed, the  $di/dt$  for the CTL circuit may be made substantially slower 20 resulting in additionally lower noise and jitter signals.

Other problems limit the LVDS system. For example, at the receiver, the LVDS 30 will drive a current  $I$  through the terminating resistor. Prior art designs sense that voltage

with a high gain amplifier. But the slew rate of the voltage signal is limited by the I/C, where C may be considerable since it is the capacitance related to the high gain amplifier required by the LVDS approach. Lowering the voltage across the terminating resistor does not help since the noise margin at the receiver will be reduced and a higher gain 5 amplifier will effectively increase capacitance and reduce bandwidths (gain bandwidth tradeoff).

Current drivers for transmission lines are known, but such systems often use a voltage sensing across the termination resistor, and as such suffer from many of the same problems associated with high gain voltage receiving amplifiers..

10 The advantages of current mode line driving are discussed in the following two articles from the IEEE Journal of Solid-State Circuits, Vol. 26, No. 4, April 1991 and Vol. 34, No. 4, April 1999, respectively entitled, "Current-Mode Techniques for High-speed VLSI circuits with Application to Current Sense Amplifier for CMOS SRAM's," and "A 1-Gb/s Bidirectional I/O Buffer Using the Current-Mode Scheme." Current 15 sensing is discussed where diode connected transistors are biased to damp ringing in the circuits. Both articles are incorporated herein by reference.

U.S. patent no. 6,476,642 B1 to Morano (Morano), filed July 2000, applies a differential current driver to drive signal buses like those found on electronic backplanes. FIG. 3 diagrams such a circuit. Here the transmission line comprises two signal lines 20 where Morano pushes a positive current I1 into one line and pulls an equal negative current I1 from the second line. Care is taken using a complex feedback bridge type circuit to balance those currents to ensure proper operation. If imbalances occur, the voltage across the Rt may be offset which may negatively affect the sensing circuit operation.

25 There has been a continuing need to design a current driving system where small currents are used and where currents are sensed at the receiver and only converted to logic voltage signals where capacitances are relatively ineffective. Relatively smaller currents can be used thus benefiting from the associated lower power and lower voltages.

## SUMMARY OF THE INVENTION

In view of the foregoing background discussion, the present invention provides a current mode transfer logic transmission line driver system and method. The inventive system provides two transmission lines each driven from unbalanced or unequal current sources. The unequal current sources are switched between the two transmission lines in response to a logic signal. The distal ends of the transmission lines share a termination resistor arranged between their signal carrying conductors. The unequal currents are sensed at the distal end, and when the unequal currents are switched between the transmission lines a different logic state is detected. The current mode driving and current sensing at the distal ends of the transmission lines, compared to voltage sensing, provide, at least, speed, power, noise and jitter advantages.

In preferred embodiments the current sensing is accomplished using diode connected MOS transistors biased at an impedance level that does not substantially affect the transmission line termination. Part of the current in each transmission line is shunted from the terminating resistor through the diode connected transistors. When the input signal logic state changes the currents shunted will change accordingly thereby indicating the new logic state.

After the current sensing at the distal ends of the transmission lines, in a preferred embodiment, the currents are independently amplified and converted into a voltage signal related to the difference between the unequal currents. The conversion to a voltage signal affords system compatibility with typical logic systems. However, the conversion to a voltage signal occurs where capacitance effects substantially do not affect the speeds, noise margins, or jitter of the received logic signal. In another embodiment, a differential current may be sensed, amplified and then converted into a voltage signal.

In practice the unequal currents into the jointly terminated transmission lines will return a current equal to the difference between the two currents through the shields or return current paths of the two transmission lines. In one embodiment a single twisted pair cable is used for signal transmission. In this case there are only the two in the cable

and no shield. First wire carries forward current equaling I while the return current I/2 returns in the second wire.

It will be appreciated by those skilled in the art that although the following Detailed Description will proceed with reference being made to illustrative embodiments, 5 the drawings, and methods of use, the present invention is not intended to be limited to these embodiments and methods of use. Rather, the present invention is of broad scope and is intended to be defined as only set forth in the accompanying claims.

## BRIEF DESCRIPTION OF THE DRAWINGS

The invention description below refers to the accompanying drawings, of which:  
10 FIGS. 1 and 3 are circuit diagrams of prior art line driver circuits,  
FIG. 2 is a signal comparison of an LVDS to a CTL circuit;  
FIG. 4A and 4B are a block diagrams of a preferred embodiments of the present invention;  
FIG. 5 is a schematic of a differential current line driver,  
15 FIG. 6 is a circuit illustrating current sensing, and  
FIG. 7 is combined schematic of a receiver circuit.

## DETAILED DESCRIPTION OF AN ILLUSTRATIVE EMBODIMENT

FIG. 4A show a diagram of a preferred embodiment of the present invention. An 20 input signal, Vin controls and selects output current signals Ia and Ib that are driven into the transmission lines 50 and 52. In one logic state Ia is a positive current out into a first transmission line 50 and Ib is a negative current in from a second transmission line 52. In the opposite logic state Ia is a negative current from the first transmission line 50 and Ib is a positive current into the second transmission line 52. In another preferred embodiment it is possible to have no current driven into either transmission line.  
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If each transmission line has a characteristic impedance of 50 ohms a 100 ohm Rt is placed across the distal ends of the signal conductors and serves to terminate both lines.

Of note is that  $I_a$  and  $I_b$  are not equal to each other so that there will be a return current through the shield. Also, since  $R_t$  is across the distal ends of both transmission lines, both ends of  $R_t$  will be biased at some positive voltage in this preferred embodiment. Preferably, in one logic state,  $I_a$  is +1 ma and  $I_b$  is -0.5 ma, whereupon there is a return current,  $I_s$ , in the shield of 0.5 ma. In the opposite logic state there still will be 0.5 ma returned through the shield.

FIG. 4B illustrates another preferred embodiment using a single twisted pair as a transmission line. As in FIG. 4A,  $I_a$  and  $I_b$  are not equal to each other, and in this case the differential current will be absorbed at the current sense receiver 54.

10 In contrast to known voltage signal sensing techniques, FIGS. 4A and 4B illustrate a current sensing circuit block diagram 54 and 56. Using a current sense circuit virtually eliminates the negative effects of capacitance multiplication of high gain voltage receiving amplifiers. The current sensing is, in this preferred embodiment, configured in parallel with  $R_t$ , and is described in more detail below. A current amplification circuit 56 receives the sensed current and finally a current to voltage (I/V) converter 58 provides a CMOS out signal compatible with standard computing circuitry. The present invention creates a voltage signal well away from the terminating and sensing circuitry where the capacitance is relatively small and ineffective.

20 FIG. 5 shows one current driver circuit that may be used in accordance with the present invention. Here, when  $V_1$  is low  $P_1$  is on and  $I_1$ , 1mA, travels via  $P_1$  out as  $I_a$ . If  $V_2$  is high  $N_2$  is on and  $I_2$ , 0.5mA, travels out via  $N_2$  as a negative  $I_b$ . Reversing the logic states of  $V_1$  and  $V_2$ ,  $I_2$  travels out as a negative  $I_a$  and  $I_1$  travels out as a positive  $I_b$ . Typically,  $V_2$  is designed as the logic inverse of  $V_1$  for the above operation. However, if  $P_1$ ,  $P_2$ ,  $N_1$  and  $N_2$  are driven independently (not shown), it will be possible to 25 turn them all off leaving no current in the transmission lines. Reader should note that the no common mode feedback circuit(CMFB) is used to stabilize the common mode level of the output voltage. This circuit is typical for an LVDS style driver. CTL doesn't require CMFB due to the special receiver used at the other end. Thus we save the current consumed by the CMFB circuit reducing the total power consumption of the system.

FIG. 6 is a schematic of a current sensing circuitry consistent with a preferred embodiment of the present invention. Here two diode connected NMOS transistors, N3 and N4, are biased to siphon off I3 and I4, respectively, from currents in the transmission lines. N3 and N4 may be biased (not shown) along the diode-like curve to overcome any threshold and to present an impedance substantially greater than  $R_t$  to minimally affect the termination of the transmission lines. In one preferred embodiment N3 and N4 exhibit about 1 K ohms each, although other impedances can be used as known in the art. If N3 and N4 present about 2 K ohms across an equivalent 100 ohm transmission line, the  $R_t$  can be made equal to 105 ohms or appropriately higher or lower to maintain proper transmission line termination. However, as is known in the art, there is likely to be some harmless ringing due to some impedance mismatch even if care is taken to keep the diode transistors at a high impedance state. For example if  $R_t$  is 105 ohms across a 100 ohm transmission line, and the diode connected transistors present, for some processing reason, a very high impedances, the 5 ohm mismatch will only result in a reflection coefficient of about less than 2.5 percent.

Still referring to FIG. 6, consider that  $I_a$  is 1 ma,  $I_b$  is -0.5 ma, then the return current,  $I_s$ , will be 0.5 ma. N3 and N4 can be designed so that  $I_t$  is 0.65 ma, with N3 drawing  $I_3$  of 0.35 ma and N4 drawing  $I_4$  of 0.15 ma. The difference between  $I_3$  and  $I_4$ , or 0.2 ma, is sensed, as discussed below, to indicate a logic signal, say a logic one. The negative of that logic signal is sensed when  $I_a$  and  $I_b$  exchange current levels when the input signal to the current drive changes state. In this state  $I_3$  and  $I_4$  will exchange current levels and 0.2 ma difference is sensed as a logic zero. So a logic change from one to zero will result in 0.4 ma change in current.

FIG. 7 shows a more detailed complete receiver circuit implementation of the blocks of FIG. 4 positioned at the termination circuit end of the two transmission lines 50 and 52. The  $R_t$  is connected from Pin+ to Pin- as shown, with  $I_a$  and  $I_b$  driving the two ends of  $R_t$ , as shown in FIG. 6. FIG. 7, is a more detailed schematic of the current sense circuit 54, current amplification circuit 56, and current to voltage, I/V, circuit 58.

In FIG. 7 the current sense circuit 54 is formed by a circuit attached to each end of  $R_t$ , with a current source I5 and I6 feeding each circuit. As known in the art, these cur-

rent sources will be typically formed by biasing PMOS transistors to the positive power rail 60. The current sensing circuit for I3 includes N5 - N8. N7 and N8, and the current sensing circuit for I4 includes N5' - N8.' N7 and N7' are diode connected NMOS transistors that share equal drain currents with N8 and N8', respectively. Since N7 and N8 have the same drain current (I5) the gate to source voltage for N7 and N8 are equal, assuming matched transistors. The discussion for N5 - N7 with respect to I3 applies directly to N5' - N7' with respect to I4, and so is not repeated below. N6 is the diode connected transistor arranged with N5 forming a controlled transistorized linear resistance to bias the diode connected devices away from the knee region and thus increase the current sensitivity. Resistances of N5 and N5' are controlled by the gate voltage of N7 and N7,' respectively, which in turn depends on current in the diode connected devices N6 and N6'. Thus the current information from the sensing element (diode connected device) is used to modify the resistance of N5 or N5' such that the effective current difference between the two branches can be increased. Resistance also has a dampening effect on a high frequency noise which appears on node A and Ab. In this circuit arrangement I5, N7 and N8 control, via the mirroring effect, I3 and the voltage drops across N5 and N6, as follows. The same current will travel through N5 and N6 so that their gate to source voltages will be equal to each, and the voltage at Pin+ via the N7 mirror. In this manner the offset voltage of the diode connected N6 can be compensated and the impedance of N6 can be controlled.

The gates of N9 and N10 connect to the drain of N6, marked A, forming a current mirror. Similarly, N11 and N12 mirror the current in N6.' N10 and N12 are sized to provide amplified currents sensed by the I-V conversion circuit via B and Bb. When I3 changes, in a preferred embodiment from 0.15 ma to 0.35 ma, this change is reflected at I9 and I10 via the current mirror amplification circuit 56. I10 can be made as an amplified version of the I3 change by sizing the transistors as is known in the art. Also, P9 is arranged as a diode connected transistor and may be biased (not shown) and I10 will mirror I9 but may be amplified by sizing P10. The gate to source voltage of P10 and P9 are equal. This provides the current amplification so that I10 is an amplified version of I3. As similar circuit receives I4 and provides an amplified version at I12.

FIG. 7 item 58 shows a circuit that performs the voltage conversion. The two outputs, B and Bb, are input to the gates of N13 and N14, respectively. I13 and I14 are mirrors of I10 and I12, respectively. P13 and P14 are current mirrors. There is a full differential operation using B and Bb providing a voltage output at C that drives N15 and 5 P15 act to provide the rail to rail CMOS logic levels.

It should be understood that above-described embodiments are being presented herein as examples and that many variations and alternatives thereof are possible. Accordingly, the present invention should be viewed broadly as being defined only as set forth in the hereinafter appended claims.

10 What is claimed is: